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Pedroni, Volnei A. Circuit design and simulation with VHDL / Volnei A. Pedroni. 2nd ed. p. cm. Rev. ed. of: Circuit design with VHDL / Volnei A. Pedroni. 2004. Includes bibliographical references and index. ISBN 978-0-262-01433-5

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Exercise Solutions 5
Problem 5.4: Unsigned
adder A possible
solution is shown below
(but see the NOTE that
follows). The ports
were considered to be
of type
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conversion by specific
functions Figure 3.10 is
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