Cmos Test And Evaluation A Physical Perspective

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Introduction to IDDQ Testing Springer Science & Business Media

An efficient automatic test pattern generator for I$sb{DDQ}$ current testing of CMOS digital circuits is presented. The complete two-line bridging fault set is considered. Because of the time constraints of I$sb{DDQ}$ testing, an adaptive genetic algorithm (GA) is used to generate compact test sets. To accurately evaluate the test sets, fault grading is performed using a switch-level fault simulator and a mixed-mode electrical-level fault simulator. The test sets are compared with those generated by HITEC, a traditional gate-level test generator. Experimental results for ISCAS85 and ISCAS89 benchmark circuits are presented. The results show that for I$sb{DDQ}$ testing, the GA test sets outperform the HITEC test sets. When the test sets are truncated due to test time constraints, the fault coverages can differ by 10% or more. In addition to test generation and test evaluation, diagnosis (fault location) is also performed using both test sets. Diagnosis is performed using fault dictionaries constructed during test evaluation. In addition to the traditional full dictionary, two reduced dictionaries are also presented. The results show that the reduced dictionaries offer good size-resolution trade-offs when compared with the full dictionary.

Automatic Testing and Evaluation of Digital Integrated Circuits ASM International

This book constitutes the proceedings of the 6th International Conference on Nonlinear Speech Processing, NOLISP 2013, held in Mons, Belgium, in June 2013. The 27 refereed papers included in this volume were carefully reviewed and selected from 34 submissions. The paper are organized in topical sections on speech and audio analysis; speech synthesis; speech-based biomedical applications; automatic speech recognition; and speech enhancement.

ISTFA 2019: Proceedings of the 45th International Symposium for Testing and Failure Analysis Springer Science & Business Media

Includes bibliographical references and index.

Wafer Level Reliability of Advanced CMOS Devices and Processes CRC Press

Developed by the Electronic Device Failure Analysis Society (EDFAS) Publications Committee.

Thirty-fourth International

Symposium for Testing and Failure Analysis Springer Science & Business Media
The increasing application of integrated circuits in situations where high reliability is needed places a requirement on the manufacturer to use methods of testing to eliminate devices that may fail on service. One possible approach that is described in this book is to make precise electrical measurements that may reveal those devices more likely to fail. The measurements assessed are of analog circuit parameters which, based on a knowledge of failure mechanisms, may indicate a future failure. . To incorporate these tests into the functional listing of very large scale integrated circuits consideration has to be given to the sensitivity of the tests where small numbers of devices may be defective in a complex circuit. In addition the tests ideally should require minimal extra test time. A range of tests has been evaluated and compared with simulation used to assess the sensitivity of the measurements. Other work in the field is fully referenced at the end of each chapter. The team at Lancaster responsible for this book wish to thank the Alvey directorate and SERe for the necessary support and encouragement to publish our results. We would also like to thank John Henderson, recently retired from the British Telecom Research Laboratories, for his cheerful and enthusiastic encouragement. Trevor Ingham, now in New Zealand, is thanked for his early work on the project.

IDDQ Testing of VLSI Circuits Springer Science & Business Media
A pragmatic approach to testing electronic systems As we move ahead in the electronic age, rapid changes in technology pose an ever-increasing number of challenges in testing electronic products. Many practicing engineers are involved in this arena, but few have a chance to study the field in a systematic way-learning takes place on the job. By covering the fundamental disciplines in detail, Principles of Testing Electronic Systems provides design engineers with the much-needed knowledge base. Divided into five major parts, this highly useful reference relates design and tests to the development of reliable electronic products; shows the main vehicles for design verification; examines designs that facilitate testing; and investigates how testing is applied to random logic, memories, FPGAs, and microprocessors. Finally, the last part offers coverage of advanced test solutions for today's very deep submicron designs. The authors take a phenomenological approach to the subject matter while providing readers with plenty of opportunities to explore the foundation in detail. Special features include: * An explanation of where a test belongs in the design flow * Detailed discussion of scan-path and ordering of scan-chains * BIST solutions for embedded logic and memory blocks * Test methodologies for FPGAs * A chapter on testing system on a chip * Numerous references

The Design, Testing, and Analysis of a Comprehensive Test Pattern for Measuring CMOS/SOS Process Performance and Control Springer Science & Business Media
The definition from SEMATECH of wafer level reliability test is: a methodology to assess the reliability impact of tools and processes by testing mechanism-specific test structures under accelerated conditions during device processing. Because wafer level reliability test is the accelerated test, it owns some different characters with common long time test in terms of failure mechanisms, test procedures, life time prediction, test structures design and so on. In this book, all items of wafer level reliability of CMOS devices and processes will be discussed. The purpose of this book is to provide a good and urgently need reference on MOS device

reliability. The authors discuss how to enhance the veracity of lifetime prediction and the effects to degrade the veracity deeply. Finally, a discussion of the problems with wafer level reliability in terms of the engineering applications and research is given.

Energy Research Abstracts ASM International

The objective of this work was to determine baseline electrical parameters that could be used to evaluate a fabrication process. Two lots of wafers containing NBS-16 test chips were fabricated at a commercial vendor in a radiation-hard, CMOS/SOS process. These wafers were then returned to NBS for testing and evaluation. Testing was performed using an automated computer-controlled integrated circuit test system. Test results were evaluated using analysis techniques which provided a statistical estimate of selected parameters and identified spatial correlations between data sets. Further analysis was then performed in order to identify process irregularities. A complete description of the test results and analysis procedure can be found in the appendices.

Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits John Wiley & Sons

Provides new or expanded coverage on the latest techniques for microelectronic failure analysis. The CD-ROM includes the complete content of the book in fully searchable Adobe Acrobat format. Developed by the Electronic Device Failure Analysis Society (EDFAS) Publications Committee

ESD Testing Springer

With the evolution of semiconductor technology and global diversification of the semiconductor business, testing of semiconductor devices to systems for electrostatic discharge (ESD) and electrical overstress (EOS) has increased in importance. ESD Testing: From Components to Systems updates the reader in the new tests, test models, and techniques in the characterization of semiconductor components for ESD, EOS, and latchup. Key features: Provides understanding and knowledge of ESD models and specifications including human body model (HBM), machine model (MM), charged device model (CDM), charged board model (CBM), cable discharge events (CDE), human metal model (HMM), IEC 61000-4-2 and IEC 61000-4-5. Discusses new testing methodologies such as transmission line pulse (TLP), to very fast transmission line pulse (VF-TLP), and future methods of long pulse TLP, to ultra-fast TLP (UF-TLP). Describes both conventional testing and new testing techniques for both chip and system level evaluation. Addresses EOS testing, electromagnetic compatibility (EMC) scanning, to current reconstruction methods. Discusses latchup characterization and testing methodologies for evaluation of semiconductor technology to product testing. ESD Testing: From Components to Systems is part of the authors ' series of books on electrostatic discharge (ESD) protection; this book will be an invaluable reference for the professional semiconductor chip and system-level ESD and EOS test engineer. Semiconductor device and process development, circuit designers, quality, reliability and failure analysis engineers will also find it an essential reference. In addition, its academic treatment will appeal to both senior and graduate students with interests in semiconductor process, device physics, semiconductor testing and experimental work.

Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits ASM International

Advances in design methods

and process technologies have resulted in a continuous increase in the complexity of integrated circuits (ICs). However, the increased complexity and nanometer-size features of modern ICs make them susceptible to manufacturing defects, as well as performance and quality issues. Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations, power supply noise, crosstalk, resistive opens/bridges, and design-for-manufacturing (DfM)-related rule violations. The book also addresses testing for small-delay defects (SDDs), which can cause immediate timing failures on both critical and non-critical paths in the circuit. Overviews semiconductor industry test challenges and the need for SDD testing, including basic concepts and introductory material Describes algorithmic solutions incorporated in commercial tools from Mentor Graphics Reviews SDD testing based on "alternative methods" that explores new metrics, top-off ATPG, and circuit topology-based solutions Highlights the advantages and disadvantages of a diverse set of metrics, and identifies scope for improvement Written from the triple viewpoint of university researchers, EDA tool developers, and chip designers and tool users, this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective. The book is designed as a one-stop reference for current industrial practices, research challenges in the domain of SDD testing, and recent developments in SDD solutions.

Rapid Reliability Assessment of VLSICs Springer Science & Business Media

This volume contains a collection of papers presented at the NATO Advanced Study Institute on · Testing and Diagnosis of VLSI and ULSI" held at Villa Olmo, Como (Italy) June 22 -July 3,1987. High Density technologies such as Very-Large Scale Integration (VLSI), Wafer Scale Integration (WSI) and the not-so-far promises of Ultra-Large Scale Integration (ULSI), have exasperated the problema associated with the testing and diagnosis of these devices and systema. Traditional techniques are fast becoming obsolete due to unique requirements such as limited controllability and observability, increasing execution complexity for test vector generation and high cost of fault simulation, to mention just a few. New approaches are imperative to achieve the highly sought goal of the · three months · turn around cycle time for a state-of-the-art computer chip. The importance of testing and diagnostic processes is of primary importance if costs must be kept at acceptable levels. The objective of this NATO-ASI was to present, analyze and discuss the various facets of testing and diagnosis with respect to both theory and practice. The contents of this volume reflect the diversity of approaches currently available to reduce test and diagnosis time. These approaches are described in a concise, yet clear way by renowned experts of the field. Their contributions are aimed at a wide readership: the uninitiated researcher will find the tutorial chapters very rewarding. The expert wiII be introduced to advanced techniques in a very comprehensive manner.

Advances in Nonlinear Speech Processing Springer Science & Business Media

The theme for the 2019 conference is Novel Computing Architectures. Papers will include discussions on the advent of Artificial Intelligence and the promise of quantum computing that are driving disruptive computing architectures; Neuromorphic chip designs on one hand, and Quantum Bits on the other, still in R&D, will introduce new computing circuitry and memory elements, novel materials, and different test methodologies. These novel computing architectures will require further innovation which is best achieved through a collaborative Failure Analysis community composed of chip manufacturers, tool vendors, and universities.

Testing for Small-Delay Defects

in Nanoscale CMOS Integrated Circuits ASM International
Microelectronic Test Structures for CMOS Technology and Products addresses the basic concepts of the design of test structures for incorporation within test-vehicles, scribe-lines, and CMOS products. The role of test structures in the development and monitoring of CMOS technologies and products has become ever more important with the increased cost and complexity of development and manufacturing. In this timely volume, IBM scientists Manjul Bhushan and Mark Ketchen emphasize high speed characterization techniques for digital CMOS circuit applications and bridging between circuit performance and characteristics of MOSFETs and other circuit elements. Detailed examples are presented throughout, many of which are equally applicable to other microelectronic technologies as well. The authors ' overarching goal is to provide students and technology practitioners alike a practical guide to the disciplined design and use of test structures that give unambiguous information on the parametrics and performance of digital CMOS technology.
NASA Technical Paper Springer
The Electronic Device Failure Analysis Society proudly announces the Seventh Edition of the Microelectronics Failure Analysis Desk Reference, published by ASM International. The new edition will help engineers improve their ability to verify, isolate, uncover, and identify the root cause of failures. Prepared by a team of experts, this updated reference offers the latest information on advanced failure analysis tools and techniques, illustrated with numerous real-life examples. This book is geared to practicing engineers and for studies in the major area of power plant engineering. For non-metallurgists, a chapter has been devoted to the basics of material science, metallurgy of steels, heat treatment, and structure-property correlation. A chapter on materials for boiler tubes covers composition and application of different grades of steels and high temperature alloys currently in use as boiler tubes and future materials to be used in supercritical, ultra-supercritical and advanced ultra-supercritical thermal power plants. A comprehensive discussion on different mechanisms of boiler tube failure is the heart of the book. Additional chapters detailing the role of advanced material characterization techniques in failure investigation and the role of water chemistry in tube failures are key contributions to the book.
CMOS Test and Evaluation Springer Science & Business Media
Testing Static Random Access Memories covers testing of one of the important semiconductor memories types; it addresses testing of static random access memories (SRAMs), both single-port and multi-port. It contributes to the technical acknowledge needed by those involved in memory testing, engineers and researchers. The book begins with outlining the most popular SRAMs architectures. Then, the description of realistic fault models, based on defect injection and SPICE simulation, are introduced. Thereafter, high quality and low cost test patterns, as well as test strategies for single-port, two-port and any p-port SRAMs are presented, together with some preliminary test results showing the importance of the new tests in reducing DPM level. The impact of the port restrictions (e.g., read-only ports) on the fault models, tests, and test strategies is also discussed. Features: -Fault primitive based analysis of memory faults, -A complete framework of and classification memory faults, -A systematic way to develop optimal and high quality memory test algorithms, -A systematic way to develop test patterns for any multi-port SRAM, -Challenges

and trends in embedded memory testing.

Microelectronic Failure Analysis Desk Reference Springer Science & Business Media

This book discusses in detail the correlation between physical defects and logic faults, and shows you how Iddq testing locates these defects. The book provides planning guidelines and optimization methods and is illustrated with numerous examples ranging from simple circuits to extensive case studies.

Principles of Testing Electronic Systems Springer

Device testing represents the single largest manufacturing expense in the semiconductor industry, costing over $40 billion a year. The most comprehensive and wide ranging book of its kind, Testing of Digital Systems covers everything you need to know about this vitally important subject. Starting right from the basics, the authors take the reader through automatic test pattern generation, design for testability and built-in self-test of digital circuits before moving on to more advanced topics such as IDDQ testing, functional testing, delay fault testing, memory testing, and fault diagnosis. The book includes detailed treatment of the latest techniques including test generation for various fault models, discussion of testing techniques at different levels of integrated circuit hierarchy and a chapter on system-on-a-chip test synthesis. Written for students and engineers, it is both an excellent senior/graduate level textbook and a valuable reference.

Test Generation and Evaluation for Bridging Faults in CMOS VLSI Circuits

ASM International

Model based testing is the most powerful technique for testing hardware and software systems. Models in Hardware Testing describes the use of models at all the levels of hardware testing. The relevant fault models for nanoscaled CMOS technology are introduced, and their implications on fault simulation, automatic test pattern generation, fault diagnosis, memory testing and power aware testing are discussed. Models and the corresponding algorithms are considered with respect to the most recent state of the art, and they are put into a historical context by a concluding chapter on the use of physical fault models in fault tolerance.

Microelectronic Failure Analysis Cambridge University Press

CMOS manufacturing environments are surrounded with symptoms that can indicate serious test, design, or reliability problems, which, in turn, can affect the financial as well as the engineering bottom line. This book educates readers, including non-engineers involved in CMOS manufacture, to identify and remedy these causes. This book instills the electronic knowledge that affects not just design but other important areas of manufacturing such as test, reliability, failure analysis, yield-quality issues, and problems. Designed specifically for the many non-electronic engineers employed in the semiconductor industry who need to reliably manufacture chips at a high rate in large quantities, this is a practical guide to how CMOS electronics work, how failures occur, and how to diagnose and avoid them. Key features: Builds a grasp of the basic electronics of CMOS integrated circuits and then leads the reader further to understand the mechanisms of failure. Unique descriptions of circuit failure mechanisms, some found previously only in research papers and others new to this publication. Targeted to the CMOS industry (or students headed there) and not a generic introduction to the broader field of electronics. Examples, exercises, and problems are provided to support the self-instruction of the reader.