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ESE570 Digital VLSI Circuits - Penn Engineering
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Consider an nMOS transistor in a 0.6 μm process with $W/L = 4/2$ (i.e., $1.2/0.6 \mu\text{m}$). In this process, the gate oxide thickness is 100 Å and the mobility of electrons is 350 cm^2/Vs .
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SOLUTIONS 14 searching.)
Silver has better conductivity than copper and gold while having poorer conductivity than copper, has good immunity to oxidization. The reason for not using gold or silver is that they both have the property that they can migrate and enter the silicon. This alters CMOS device characteristics in undesirable ways.
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effort should be about 4. This

design has imbalanced delays
and excessive efforts. The path
effort is $F = 12 * 6 * 9 = 648$.
The best number of stages is 4
or 5. One way to speed the
circuit up is to add a buffer
(two inverters) at the end. The
gates should be resized to bear
efforts of $f = 648^{1/5} = 3.65$
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