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The Hardware Software Interface Technical Publications

A new approach to the study of arithmetic circuits In Synthesis of Arithmetic Circuits: FPGA, ASIC and EmbeddedSystems, the authors take a novel approach of presenting methodsand examples for the synthesis of arithmetic circuits that betterreflects the needs of today's computer system designers andengineers. Unlike other publications that limit discussion toarithmetic units for general-purpose computers, this text featuresa practical focus on embedded systems. Following an introductory chapter, the publication is divided intotwo parts. The first part, Mathematical Aspects and Algorithms,includes mathematical background, number representation, additionand subtraction, multiplication, division, other arithmeticoperations, and operations in finite fields. The second part,Synthesis of Arithmetic Circuits, includes hardware platforms,general principles of synthesis, adders and subtractors,multipliers, dividers, and other arithmetic primitives. Inaddition, the publication distinguishes itself with: * A separate treatment of algorithms and circuits-a more usefulpresentation for both software and hardware implementations * Complete executable and synthesizable VHDL models available onthe book's companion Web site, allowing readers to generatesynthesizable descriptions * Proposed FPGA implementation examples, namely synthesizablelow-level VHDL models for the Spartan II and Virtex families * Two chapters dedicated to finite field operations This publication is a must-have resource for students in computerscience and embedded system designers, engineers, and researchersin the field of hardware and software computer system design anddevelopment. An Instructor Support FTP site is available from the Wileyeditorial department.

Instructor's Manual For Computer Arithmetic McGraw-Hill Education

This title provides a view of computer arithmetic, covering topics in arithmetic unit design and circuit implementation that complement the architectural and algorithmic speedup techniques used in high-performance computer architecture and parallel processing.

FPGA, ASIC and Embedded Systems Morgan & Claypool Publishers

Ideal for graduate and

senior undergraduate courses in computer arithmetic and advanced digital design, Computer Arithmetic: Algorithms and Hardware Designs, Second Edition, provides a balanced, comprehensive treatment of computer arithmetic. It covers topics in arithmetic unit design and circuit implementation that complement the architectural and algorithmic speedup techniques used in high-performance computer architecture and parallel processing. Using a unified and consistent framework, the text begins with number representation and proceeds through basic arithmetic operations, floating-point arithmetic, and function evaluation methods. Later chapters cover broad design and implementation topics-including techniques for high-throughput, low-power, fault-tolerant, and reconfigurable arithmetic. An appendix provides a historical view of the field and speculates on its future. An indispensable resource for instruction, professional development, and research, Computer Arithmetic: Algorithms and Hardware Designs, Second Edition, combines broad coverage of the underlying theories of computer arithmetic with numerous examples of practical designs, worked-out examples, and a large collection of meaningful problems. This second edition includes a new chapter on reconfigurable arithmetic, in order to address the fact that arithmetic functions are increasingly being implemented on field-programmable gate arrays (FPGAs) and FPGA-like configurable devices. Updated and thoroughly revised, the book offers new and expanded coverage of saturating adders and multipliers, truncated multipliers, fused multiply-add units, overlapped quotient digit selection, bipartite and multipartite tables, reversible logic, dot notation, modular arithmetic, Montgomery modular reduction, division by constants, IEEE floating-point standard formats, and interval arithmetic. Features: * Divided into 28 lecture-size chapters * Emphasizes both the underlying theories of computer arithmetic and actual hardware designs * Carefully links computer arithmetic to other subfields of computer engineering * Includes 717 end-of-chapter problems ranging in complexity from simple exercises to mini-projects * Incorporates many examples of practical designs * Uses consistent standardized notation throughout * Instructor's manual includes solutions to text problems * An author-maintained website http: //www.ece.ucsb.edu/ parhami/text comp arit.htm contains instructor resources, including complete lecture slides

Computer Organization and Design RISC-V Edition Tata McGraw-Hill Education

Foreword -- Foreword to the First Printing -- Preface -- Chapter 1 -- Introduction --

Chapter 2 -- Message Switching Layer -- Chapter 3 -- Deadlock, Livelock, and Starvation -- Chapter 4 -- Routing Algorithms -- Chapter 5 -- CollectiveCommunicationSupport -- Chapter 6 -- Fault-Tolerant Routing -- Chapter 7 -- Network Architectures -- Chapter 8 -- Messaging Layer Software -- Chapter 9 -- Performance Evaluation -- Appendix A -- Formal Definitions for Deadlock Avoidance -- Appendix B -- Acronyms -- References -- Index.

From Microprocessors to Supercomputers John Wiley & Sons

This textbook is designed for the first course in Computer Architecture, usually offered at the junior/senior (3rd, 4th year) level in electrical engineering, computer science or computer engineering departments. This course is required of all electrical engineering and computer science/computer engineering majors specializing in the design of computer systems. This text provides a comprehensive introduction to computer architecture, covering topic from design of simple microprocessors to techniques used in the most advanced supercomputers.

Fault-tolerant Computer System Design Oxford University Press, USA

Designed as an introductory text for the students of computer science, computer applications, electronics engineering and information technology for their first course on the organization and architecture of computers, this accessible, student friendly text gives a clear and in-depth analysis of the basic principles underlying the subject. This self-contained text devotes one full chapter to the basics of digital logic. While the initial chapters describe in detail about computer organization, including CPU design, ALU design, memory design and I/O organization, the text also deals with Assembly Language Programming for Pentium using NASM assembler. What distinguishes the text is the special attention it pays to Cache and Virtual Memory organization, as well as to RISC architecture and the intricacies of pipelining. All these discussions are climaxed by an illuminating discussion on parallel computers which shows how processors are interconnected to create a variety of parallel computers. KEY FEATURES Self-contained presentation starting with data representation and ending with advanced parallel computer architecture. Systematic and logical organization of topics. Large number of worked-out examples and exercises. Contains basics of assembly language programming. Each chapter has learning objectives and a detailed summary to help students to quickly revise the material.

Algorithms and Hardware Designs Instructor's Manual for Computer for Arithmetic PHI Learning Pvt. Ltd.

Ideal for graduate and senior undergraduate courses in computer arithmetic and advanced digital design, Computer Arithmetic: Algorithms and Hardware Designs, Second Edition, provides a balanced, comprehensive treatment of computer arithmetic. It covers topics in arithmetic unit design and circuit implementation that complement the architectural and algorithmic speedup techniques used in high-performance computer architecture and parallel processing. Using a unified and consistent framework, the text begins with number representation and proceeds through basic arithmetic operations, floating-point arithmetic, and function evaluation methods. Later chapters cover broad design and implementation topics-including techniques for high-throughput, low-power, fault-tolerant, and reconfigurable arithmetic. An appendix provides a historical view of the field and speculates on its future.An indispensable resource for instruction, professional development, and research, Computer

Arithmetic: Algorithms and Hardware Designs, Second Edition, combines broad coverage of the underlying theories of computer arithmetic with numerous examples of practical designs, worked-out examples, and a large collection of meaningful problems. This second edition includes a new chapter on reconfigurable arithmetic, in order to address the fact that arithmetic functions are increasingly being implemented on field-programmable gate arrays (FPGAs) and FPGA-like configurable devices. Updated and thoroughly revised, the book offers new and expanded coverage of saturating adders and multipliers, truncated multipliers, fused multiply-add units, overlapped quotient digit selection, bipartite and multipartite tables, reversible logic, dot notation, modular arithmetic, Montgomery modular reduction, division by constants, IEEE floating-point standard formats, and interval arithmetic.Readership: Graduate and senior undergraduate courses in computer arithmetic and advanced digital design.

Fault Tolerance, Analysis, and Design John Wiley & Sons

The new RISC-V Edition of Computer Organization and Design features the RISC-V open source instruction set architecture, the first open source architecture designed to be used in modern computing environments such as cloud computing, mobile devices, and other embedded systems. With the post-PC era now upon us, Computer Organization and Design moves forward to explore this generational change with examples, exercises, and material highlighting the emergence of mobile computing and the Cloud. Updated content featuring tablet computers, Cloud infrastructure, and the x86 (cloud computing) and ARM (mobile computing devices) architectures is included. An online companion Web site provides advanced content for further study, appendices, glossary, references, and recommended reading. Features RISC-V, the first such architecture designed to be used in modern computing environments, such as cloud computing, mobile devices, and other embedded systems Includes relevant examples, exercises, and material highlighting the emergence of mobile computing and the cloud

Basic Computer Architecture Cambridge University Press

This textbook introduces readers to assembly and its role in computer programming and design. The author concentrates on covering the 8086 family of processors up to and including the Pentium. The focus is on providing students with a firm grasp of the main features of assembly programming, and how it can be used to improve a computer's performance. All of the main features are covered in depth: stacks, addressing modes, arithmetic, selection and iteration, as well as bit manipulation. Advanced topics include: string processing, macros, interrupts and input/output handling, and interfacing with such higher-level languages as C. The book is based on a successful course given by the author and includes numerous hands-on exercises.

Software Testing and Quality Assurance Morgan & Claypool Publishers

Arabic Type-Making in the Machine Age is an in-depth historical study of the evolution of Arabic type under the influence of changing technologies in the

twentieth century.

Multi-Core Cache Hierarchies Springer Science & Business Media

The Encyclopedia of Big Data Technologies provides researchers, educators, students and industry professionals with a comprehensive authority over the most relevant Big Data Technology concepts. With over 300 articles written by worldwide subject matter experts from both industry and academia, the encyclopedia covers topics such as big data storage systems, NoSQL database, cloud computing, distributed systems, data processing, data management, machine learning and social technologies, data science. Each peer-reviewed, highly structured entry provides the reader with basic terminology, subject overviews, key research results, application examples, future directions, cross references and a bibliography. The entries are expository and tutorial, making this reference a practical resource for students, academics, or professionals. In addition, the distinguished, international editorial board of the encyclopedia consists of well-respected scholars, each developing topics based upon their expertise.

Algorithms and Architectures CRC Press

A key determinant of overall system performance and power dissipation is the cache hierarchy since access to off-chip memory consumes many more cycles and energy than on-chip accesses. In addition, multi-core processors are expected to place ever higher bandwidth demands on the memory system. All these issues make it important to avoid off-chip memory access by improving the efficiency of the on-chip cache. Future multi-core processors will have many large cache banks connected by a network and shared by many cores. Hence, many important problems must be solved: cache resources must be allocated across many cores, data must be placed in cache banks that are near the accessing core, and the most important data must be identified for retention. Finally, difficulties in scaling existing technologies require adapting to and exploiting new technology constraints. The book attempts a synthesis of recent cache research that has focused on innovations for multi-core processors. It is an excellent starting point for early-stage graduate students, researchers, and practitioners who wish to understand the landscape of recent cache research. The book is suitable as a reference for advanced computer architecture classes as well as for experienced researchers and VLSI engineers. Table of Contents: Basic Elements of Large Cache Design / Organizing Data in CMP Last Level Caches / Policies Impacting Cache Hit Rates / Interconnection Networks within Large Caches / Technology / Concluding Remarks

Your Brain Is a Time Machine: The Neuroscience and Physics of Time OUP USA

This book is a comprehensive text on basic, undergraduate-level computer architecture. It starts from theoretical preliminaries and simple Boolean algebra. After a quick discussion on logic gates, it describes three classes of assembly languages: a custom RISC ISA called SimpleRisc, ARM, and x86. In the next part, a processor is designed for the SimpleRisc ISA from scratch. This includes the combinational units, ALUs, processor, basic 5-stage pipeline, and a microcode-based design. The last part of the book discusses caches, virtual memory, parallel programming, multiprocessors, storage devices and modern I/O systems. The book's website has links to slides for each chapter and video lectures hosted on YouTube.

Advanced Computer Architecture, 3e Computer ArchitectureFrom Microprocessors to Supercomputers

"Beautifully written, eloquently reasoned···Mr. Buonomano takes us off and running on an edifying scientific journey." —Carol Tavris, Wall Street Journal In Your Brain Is a Time Machine, leading neuroscientist Dean Buonomano embarks on an

"immensely engaging" exploration of how time works inside the brain (Barbara Kiser, Nature). The human brain, he argues, is a complex system that not only tells time, but creates it; it constructs our sense of chronological movement and enables "mental time travel"—simulations of future and past events. These functions are essential not only to our daily lives but to the evolution of the human race: without the ability to anticipate the future, mankind would never have crafted tools or invented agriculture. This virtuosic work of popular science will lead you to a revelation as strange as it is true: your brain is, at its core, a time machine.

Synthesis of Arithmetic Circuits Springer Science & Business Media

With computers becoming embedded as controllers in everything fromnetwork servers to the routing of subway schedules to NASAmissions, there is a critical need to ensure that systems continueto function even when a component fails. In this book, bestsellingauthor Martin Shooman draws on his expertise in reliabilityengineering and software engineering to provide a complete andauthoritative look at fault tolerant computing. He clearly explainsall fundamentals, including how to use redundant elements in systemdesign to ensure the reliability of computer systems andnetworks. Market: Systems and Networking Engineers, Computer Programmers, ITProfessionals.

Digital Arithmetic John Wiley & Sons

THE CONTEXT OF PARALLEL PROCESSING The field of digital computer architecture has grown explosively in the past two decades. Through a steady stream of experimental research, tool-building efforts, and theoretical studies, the design of an instruction-set architecture, once considered an art, has been transformed into one of the most quantitative branches of computer technology. At the same time, better understanding of various forms of concurrency, from standard pipelining to massive parallelism, and invention of architectural structures to support a reasonably efficient and user-friendly programming model for such systems, has allowed hardware performance to continue its exponential growth. This trend is expected to continue in the near future. This explosive growth, linked with the expectation that performance will continue its exponential rise with each new generation of hardware and that (in stark contrast to software) computer hardware will function correctly as soon as it comes off the assembly line, has its down side. It has led to unprecedented hardware complexity and almost intolerable dev- opment costs. The challenge facing current and future computer designers is to institute simplicity where we now have complexity; to use fundamental theories being developed in this area to gain performance and ease-of-use benefits from simpler circuits; to understand the interplay between technological capabilities and limitations, on the one hand, and design decisions based on user and application requirements on the other.

Computer Arithmetic Algorithms Springer Science & Business Media

A team of recognized experts leads the way to dependable computing systems With computers and networks pervading every aspect of

daily life, there is an ever-growing demand for dependability. In this unique resource, researchers and organizations will find the tools needed to identify and engage state-of-the-art approaches used for the specification, design, and assessment of dependable computer systems. The first part of the book addresses models and paradigms of dependable computing, and the second part deals with enabling technologies and applications. Tough issues in creating dependable computing systems are also tackled, including: Verification techniques Model-based evaluation Adjudication and data fusion Robust communications primitives Fault tolerance Middleware Grid security Dependability in IBM mainframes Embedded software Real-time systems Each chapter of this contributed work has been authored by a recognized expert. This is an excellent textbook for graduate and advanced undergraduate students in electrical engineering, computer engineering, and computer science, as well as a must-have reference that will help engineers, programmers, and technologists develop systems that are secure and reliable.

Electromagnetic Waves Elsevier

The merging of computer and communication technologies with consumer electronics has opened up new vistas for a wide variety of designs of computing systems for diverse application areas. This revised and updated third edition on Computer Organization and Design strives to make the students keep pace with the changes, both in technology and pedagogy in the fast growing discipline of computer science and engineering. The basic principles of how the intended behaviour of complex functions can be realized with the interconnected network of digital blocks are explained in an easy-to-understand style. WHAT IS NEW TO THIS EDITION : Includes a new chapter on Computer Networking, Internet, and Wireless Networks. Introduces topics such as wireless input-output devices, RAID technology built around disk arrays, USB, SCSI, etc. Key Features Provides a large number of design problems and their solutions in each chapter. Presents state-of-the-art memory technology which includes EEPROM and Flash Memory apart from Main Storage, Cache, Virtual Memory, Associative Memory, Magnetic Bubble, and Charged Couple Device. Shows how the basic data types and data structures are supported in hardware. Besides students, practising engineers should find reading this design-oriented text both useful and rewarding.

Architecture, Reconfiguration, and Modeling Elsevier

The authors provide an introduction to quantum computing. Aimed at advanced undergraduate and beginning graduate students in these disciplines, this text is illustrated with diagrams and exercises.

Algorithms and Hardware Designs Ronald M. Rothenberg

The authoritative reference on the theory and design practice of computer arithmetic.