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follows: RegWrite MemRead ALUMux MemWrite ALUOp RegMux
Branch a. 1 0 0 (Reg) 0 Add 1 (ALU) 0 b. 1 1 1 (Imm) 0 Add 1
(Mem) 0 ALUMux is the control signal that controls the Mux at the
ALU input, 0 (Reg) selects the output of the register ? le and 1
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organisms and computer networks is shown. It can be
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