

# Conformal Lec User Manual

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[Practical ECOs using Conformal ECO tool - Cadence](#)

Page 1 ENCOUNTER CONFORMAL EQUIVALENCE CHECKER Cadence Encounter Conformal Equivalence Checker (EC), ® ® ® makes it possible to verify and debug multi-million-gate designs without using test vectors. It offers the only complete equivalence checking solution available for verifying SoC designs—from RTL to final LVS netlist (SPICE)—as well as FPGA designs.

## [17. Cadence Encounter Conformal Support](#)

Cadence Encounter Conformal Equivalence Checking User Guide (LEC) 3. User -manual-cadence Design Systems- Encounter Conformal Equivalence. PDF | In this paper we will explore how to use the Cadence Conformal LEC tool capabilities to verify different types of designs, based on the.

[Can I've a link for the user guide of cadence encounter ...](#)

Cadence Conformal suite of tools contains a tool called Logic Equivalence Checker or LEC. Section 4 of this tutorial describes how to formally verify that the synthesized design is functionally equivalent to the RTL description using LEC. This section can be skipped if one chooses to use Formality for equivalence checking. During the ...

Conformal Lec User Manual

Initial command file, .conformal\_lec, executed in the following order (3.4.0.a or later): ... User Manual: PDF format file with information related to the product (for example; installation, process flow, and GUI)

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CONFORMAL LEC TUTORIAL PDF - This is a brief introduction on how to using Conformal LEC tool for your IC design. This tutorial provides a quick getting-strated guide to Cadence

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[Computer-Aided VLSI System Design - ??????](#)

Equivalence Checking Using Cadence Conformal LEC Formal Hardware

Verification ... CONFORMAL-LEC Preferences Window LEC> add

compared points —all LEC> compare LEC> Compare done! Compared points

Equi ent Non—equi u al ent T -VHDL —Rev i sed

[Conformal LEC failures debug by using Gates On the Fly](#)

1 The Conformal LEC software does not support the

read\_comments\_as\_HDL synthesis directive, and the directive

does not affect the Conformal LEC software. Table 17–1 lists

supported pragmas and trigger keywords for formal verification. c

Do not use Verilog 2001-style pragma declarations. The Quartus

II software and the

Gates On the Fly Use Case: Conformal LEC failures debug  
www.nandigits.com Conformal LEC schematic Conformal LEC  
GUI debug tool gave some useful information, but not sufficient  
and efficient. The schematic from LEC debug tool printed out too  
many gates and connections. The culprit gates were hiding  
somewhere.

**Digital Logic Synthesis and Equivalence Checking Tools ...**

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Cadence ® Conformal ® Equivalence Checker (EC) makes it possible  
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vectors. It offers the industry's only complete equivalence checking  
solution for verifying SoC designs—from RTL to final LVS netlist  
(SPICE)—as well as FPGA designs.

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CADENCE CONFORMAL LEC USER GUIDE PDF - 22 Jun If you  
didn't know, Conformal's very own AE team put together some cool  
request, technical documentation, solutions and more in your  
personalized. Jan 5, 2019. CADENCE CONFORMAL LEC USER  
GUIDE PDF. By admin inLiterature.

[Equivalence Checking Using Cadence Conformal LEC](#)

Best known methods for using Cadence Conformal LEC at Intel 3  
The design that we use as our test case is a high-performance,  
dual-port gigabit Ethernet controller for servers and embedded  
system design [7].

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See if this can help you 1. <http://users.encs.concordia.ca/~tahar/co>

[en7501/notes/lec-slides10.pdf](#) 2. Cadence Encounter Conformal  
Equivalence Checking User Guide (LEC ...

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CADENCE CONFIDENTIAL 1 CADENCE DESIGN SYSTEMS, INC.

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Conformal ECO Steps R1 vs R2 • Compare LEC golden RTL and

Modified RTL. • Review the non-equivalence points. R1 vs

LAY1 •Compare Golden PNR netlist with original RTL. This

should be clean. R2 vs G2 •New RTL with ECO fix compared

with synthesized netlist of R2 for equivalence. This should be

clean. LAY1 vs G2 •Non-equivalence expected.

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Computer-Aided VLSI System Design EC Lab : Design Verification

(Fall, Nov. 2010) ===== Motivation and Importance of Equivalence

Checking As a golden model is constructed, we prefer to check the

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equivalence between golden model ... To understand how to use  
Conformal LEC to formally check the equivalence between your VLSI  
designs in the design ...

*Conformal LEC - vsevteme.ru*

(TXT) (TXT), cadence-conformal-lec-user-manual.html, 03-Sep-2015  
20:15, 9.1K. (TXT). Encounter/Conformal). The SKILL code The  
generated user interfaces guide the engineer through com- pleting the  
greyed out “Insert Scan”, “LEC” and “STA” buttons), but This form