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Lecture 4: Digital Logic Gates ??? ?????? ?????? - ??? ??????????Q. 5.6: A sequential circuit with two D flip-flops A and B, two inputs, x and y; and one output z is Q. 5.1: The D latch of Fig. 5.6 is constructed with four NAND gates and an inverter. Consider the Digital Logic Design - Unit 04 - Combinational Logic - Part 03 - Design Procedure Q. 3.6: Simplify the following Boolean expressions, using four-variable maps: (a) A'B'C'D' + AC'D' + Q. 4.37: Implement the following Boolean function with a 4 * 1 multiplexer and external gates Q. 4.35: Implement a full adder with two 4 * 1 multiplexers.

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