On Chip ESD Protection For Integrated Circuits An IC Design Perspective

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Information Systems Design and Intelligent Applications John Wiley & Sons

Simulation Methods for ESD Protection Development looks at the integration of new techniques into a comprehensive development flow, which is now available due advances made in the field during the recent years. These findings allow for an early, stable ESD concept at a very early stage of the technology development, which is essential now development cycles have been reduced. The book also offers ways of increasing the optimization and control of the technology concerning performance, thus making the process more cost effective and increasingly efficient. This title provides a guide through the latest research and technology presenting the ESD protection development methodology. This is based on a combination of process, device and circuit stimulation, and addresses the optimization of the industry critical issue, reduced development cycles.Written to address the needs

of the ESD engineer, this text is required reading by all industry practitioners and researchers and students within this field. The FIRST Extensive overview on the subject of ESD simulation Addresses the industry critical issue of reduced development cycles, and provides solutions Presents the latest research in the field with high practical relevance and its results

ESD Protection Device and Circuit Design for Advanced CMOS Technologies John Wiley & Sons

Mixed-Signal Circuits offers a thoroughly modern treatment of integrated circuit design in the context of mixed-signal applications. Featuring chapters authored by leading experts from industry and academia, this book: Discusses signal integrity and large-scale simulation, verification, and testing Demonstrates advanced design techniques that enable digital circuits and sensitive analog circuits to coexist without any compromise Describes the process technology needed to address the performance challenges associated with developing complex mixed-signal circuits Deals with modeling topics, such as reliability, variability, and crosstalk, that define pre-silicon design methodology and trends, and are the focus of companies involved in wireless applications Develops methods to move analog into the digital domain quickly, minimizing and eliminating common trade-offs between performance, power consumption, simulation time, verification, size, and cost Details approaches for very low-power performances, high-speed interfaces, phase-locked loops (PLLs), voltage-controlled oscillators (VCOs), analog-to-digital converters (ADCs), and biomedical filters Delineates the respective parts of a full system-on-chip (SoC), from the digital parts to the baseband blocks, radio frequency (RF) circuitries, electrostatic-discharge (ESD) structures, and built-in self-test (BIST) architectures Mixed-Signal Circuits explores exciting opportunities in wireless communications and beyond. The book is a must for anyone involved in mixed-signal circuit design for future technologies.

Practical ESD Protection Design John Wiley & Sons

As we enter the nanoelectronics era, electrostatic discharge (ESD) phenomena is an important issue for everything from micro-electronics to nanostructures. This book provides insight into the operation and design of micro-gaps and nanogenerators with chapters on low capacitance ESD design in advanced technologies, electrical breakdown in micro-gaps, nanogenerators from ESD, and theoretical prediction and optimization of triboelectric nanogenerators. The information contained herein will prove useful for for engineers and scientists that have an interest in ESD physics and design.

Basic ESD and I/O Design John Wiley & Sons

A comprehensive and in-depth review of analog circuitlayout, schematic architecture, device, power network and ESDdesign This book will provide a balanced overview of analog circuitdesign layout, analog circuit schematic development,architecture of chips, and ESD design. It will start atan introductory level and will bring the reader right up to thestate-of-the-art. Two critical design aspects for analog and powerintegrated circuits are combined. The first design aspect coversanalog circuit design techniques to achieve the desired circuitperformance. The second and main aspect presents the additionalchallenges associated with the design of adequate and effective ESDprotection elements and schemes. A comprehensive list of practicalapplication examples is used to demonstrate the successfulcombination of both techniques and any potential designtrade-offs. Chapter One looks at analog design discipline, including layoutand analog matching and analog layout design practices. Chapter Twodiscusses analog design with circuits, examining: singletransistor amplifiers; multi-transistor amplifiers; active loadsand more. The third chapter covers analog design layout (alsoMOSFET layout),

before Chapters Four and Five discuss analog designsynthesis. The next chapters introduce the reader to analog-digitalmixed signal design synthesis, analog signal pin ESD networks, andanalog ESD power clamps. Chapter Nine, the last chapter, covers ESDdesign in analog applications. Clearly describes analog design fundamentals (circuitfundamentals) as well as outlining the various ESDimplications Covers a large breadth of subjects and technologies, such asCMOS, LDMOS, BCD, SOI, and thick body SOI Establishes an “ESD analog design” discipline thatdistinguishes itself from the alternative ESD digital designfocus Focuses on circuit and circuit design applications Assessible, with the artwork and tutorial style of the ESD bookseries PowerPoint slides are available for university facultymembers Even in the world of digital circuits, analog and power circuitsare two very important but under-addressed topics, especially fromthe ESD aspect. Dr. Voldman’s new book will serve as anessential and practical guide to the greater IC community. Withhigh practical and academic values this book is a“bible” for professionals, graduate students, deviceand circuit designers for investigating the physics of ESD and forproduct designs and testing.

On-Chip ESD Protection for Integrated Circuits BoD – Books on Demand

Provides the understanding and practical skills needed to develop and maintain an effective ESD control program for manufacturing, storage, and handling of ESD sensitive components This essential guide to ESD control programs explains the principles and practice of ESD control in an easily accessible way whilst also providing more depth and a wealth of references for those who want to gain a deeper knowledge of the subject. It describes static electricity and ESD principles such as triboelectrification, electrostatic fields, and induced voltages, with the minimum of theory or mathematics. It is designed for the reader to "dip into" as required, rather than need to read cover to cover. The ESD Control Program Handbook begins with definitions and commonly used terminology, followed by the principles of static electricity and ESD control. Chapter 3 discusses ESD susceptible electronic devices, and how ESD susceptibility of a component is measured. This is followed by the “Seven habits of a highly effective ESD program”, explaining the essential activities of an effective ESD control program. While most texts mainly address manual handling of ESD susceptible devices, Chapter 5 extends the discussion to ESD control in automated systems, processes and handling, which form a major part of modern electronic manufacture. Chapter 6 deals with requirements for compliance given by the IEC 61340-5-1 and ANSI/ESD S20.20 ESD control standards. Chapter 7 gives an overview of the selection, use, care and maintenance of equipment and furniture commonly used to control ESD risks. The chapter explains how these often work together as part of a system and must be specified with that in mind. ESD protective packaging is available in an extraordinary range of forms from bags, boxes and bubble wrap to tape and reel packaging for automated processes. The principles and practice of this widely misunderstood area of ESD control are introduced in Chapter 8. The thorny question of how to evaluate an ESD control program is addressed in Chapter 9 with a goal of compliance with a standard as well as effective control of ESD risks and possible customer perceptions. Whilst evaluating an existing ESD control program provides challenges, developing an ESD control program from scratch provides others. Chapter 10 gives an approach to this. Standard test methods used in compliance with ESD control standards are explained and simple test procedures given in Chapter 11. ESD Training has long been recognised as essential in

maintaining effective ESD control. Chapter 12 discusses ways of covering essential topics and how to demonstrate static electricity in action. The book ends with a look at where ESD control may go in the near future. The ESD Control Program Handbook: Gives readers a sound understanding of the subject to analyze the ESD control requirements of manufacturing processes, and develop an effective ESD control program Provides practical knowledge, as well as sufficient theory and background to understand the principles of ESD control Teaches how to track and identify how ESD risks arise, and how to identify fitting means for minimizing or eliminating them Emphasizes working with modern ESD control program standards IEC 61340-5-1 and ESD S20:20 The ESD Control Program Handbook is an invaluable reference for anyone tasked with setting up, evaluating, or maintaining an effective ESD control program, training personnel, or making ESD control related measurements. It would form an excellent basis for a University course on the subject as well as a guide and resource for industry professionals.

ESD Testing Stanford University

Electrical Overstress (EOS) continues to impact semiconductor manufacturing, semiconductor components and systems as technologies scale from micro- to nano-electronics. This bookteaches the fundamentals of electrical overstress and how to minimize and mitigate EOS failures. The text provides a clear picture of EOS phenomena, EOS origins, EOS sources, EOS physics, EOS failure mechanisms, and EOS on-chip and system design. It provides an illuminating insight into the sources of EOS in manufacturing, integration of on-chip, and system level EOS protection networks, followed by examples in specific technologies, circuits, and chips. The book is unique in covering the EOS manufacturing issues from on-chip design and electronic design automation to factory-level EOS program management in today's modern world. Look inside for extensive coverage on: Fundamentals of electrical overstress, from EOS physics, EOS time scales, safe operating area (SOA), to physical models for EOS phenomena EOS sources in today's semiconductor manufacturing environment, and EOS program management, handling and EOS auditing processing to avoid EOS failures EOS failures in both semiconductor devices, circuits and system Discussion of how to distinguish between EOS events, and electrostatic discharge (ESD) events (e.g. such as human body model (HBM), charged device model (CDM), cable discharge events (CDM), charged board events (CBE), to system level IEC 61000-4-2 test events) EOS protection on-chip design practices and how they differ from ESD protection networks and solutions Discussion of EOS system level concerns in printed circuit boards (PCB), and manufacturing equipment Examples of EOS issues in state-of-the-art digital, analog and power technologies including CMOS, LDMOS, and BCD EOS design rule checking (DRC), LVS, and ERC electronic design automation (EDA) and how it is distinct from ESD EDA systems EOS testing and qualification techniques, and Practical off-chip ESD protection and system level solutions to provide more robust systems Electrical Overstress (EOS): Devices, Circuits and Systems is a continuation of the author's series of books on ESD protection. It is an essential reference and a useful insight into the issues that confront modern technology as we enter the nano-electronic era.

Light-Emitting Diodes John Wiley & Sons

Electrical Overstress (EOS) continues to impact semiconductor manufacturing, semiconductor components and systems as technologies scale from micro- to nano-

electronics. This bookteaches the fundamentals of electrical overstress and how to minimize and mitigate EOS failures. The text provides a clear picture of EOS phenomena, EOS origins, EOS sources, EOS physics, EOS failure mechanisms, and EOS on-chip and system design. It provides an illuminating insight into the sources of EOS in manufacturing, integration of on-chip, and system level EOS protection networks, followed by examples in specific technologies, circuits, and chips. The book is unique in covering the EOS manufacturing issues from on-chip design and electronic design automation to factory-level EOS program management in today's modern world. Look inside for extensive coverage on: Fundamentals of electrical overstress, from EOS physics, EOS time scales, safe operating area (SOA), to physical models for EOS phenomena EOS sources in today's semiconductor manufacturing environment, and EOS program management, handling and EOS auditing processing to avoid EOS failures EOS failures in both semiconductor devices, circuits and system Discussion of how to distinguish between EOS events, and electrostatic discharge (ESD) events (e.g. such as human body model (HBM), charged device model (CDM), cable discharge events (CDM), charged board events (CBE), to system level IEC 61000-4-2 test events) EOS protection on-chip design practices and how they differ from ESD protection networks and solutions Discussion of EOS system level concerns in printed circuit boards (PCB), and manufacturing equipment Examples of EOS issues in state-of-the-art digital, analog and power technologies including CMOS, LDMOS, and BCD EOS design rule checking (DRC), LVS, and ERC electronic design automation (EDA) and how it is distinct from ESD EDA systems EOS testing and qualification techniques, and Practical off-chip ESD protection and system level solutions to provide more robust systems Electrical Overstress (EOS): Devices, Circuits and Systems is a continuation of the author's series of books on ESD protection. It is an essential reference and a useful insight into the issues that confront modern technology as we enter the nano-electronic era.

On-Chip Electro-Static Discharge (ESD) Protection for Radio-Frequency Integrated Circuits Elsevier

A thorough and concise treatment of ESD Recognizing its methodic, step-by-step attack of theelectrostatic discharge (ESD) problem, the initial release of thisbook was quoted by specialists as "the most thorough and concisetreatment of the broad ESD continuum that is available." Now in itsThird Edition, this book delivers the same trusted coverageof the topic while also incorporating recent technological advancesthat have taken place in the engineering community. The book beginswith the basics of ESD for humans and objects, and goes on tocover: Effects of ESD coupled to electronics Principal ESD specifications ESD diagnostics and testing Design for ESD immunity To help with troubleshooting, many ESD case histories are givenalong with their successful fixes. Electrostatic Dischargeis essential reading for all designers who want to avoid componentfailures, no trouble found incidents, and random errors.

Electrostatic Discharge Springer

An authoritative single-volume reference on the design and

analysis of ESD protection for ICs Electrostatic discharge (ESD) is a major reliability challenge to semiconductors, integrated circuits (ICs), and microelectronic systems. On-chip ESD protection is a vital to any electronic products, such as smartphones, laptops, tablets, and other electronic devices. Practical ESD Protection Design provides comprehensive and systematic guidance on all major aspects of designs of on-chip ESD protection for integrated circuits (ICs). Written for students and practicing engineers alike, this one-stop resource covers essential theories, hands-on design skills, computer-aided design (CAD) methods, characterization and analysis techniques, and more on ESD protection designs. Detailed chapters examine an array of topics ranging from fundamental to advanced, including ESD phenomena, ESD failure analysis, ESD testing models, ESD protection devices and circuits, ESD design layout and technology effects, ESD design flows and co-design methods, ESD modelling and CAD techniques, and future ESD protection concepts. Based on the author's decades of design, research and teaching experiences, Practical ESD Protection Design: • Features numerous real-world ESD protection design examples • Emphasizes on ESD protection design techniques and procedures • Describes ESD-IC co-design methodology for high-performance mixed-signal ICs and broadband radio-frequency (RF) ICs • Discusses CAD-based ESD protection design optimization and prediction using both Technology and Electrical Computer-Aided Design (TCAD/ECAD) simulation • Addresses new ESD CAD algorithms and tools for full-chip ESD physical design verification • Explores the disruptive future outlook of ESD protection Practical ESD Protection Design is a valuable reference for industrial engineers and academic researchers in the field, and an excellent textbook for electronic engineering courses in semiconductor microelectronics and integrated circuit designs.

Nano-CMOS Circuit and Physical Design John Wiley & Sons

Interest in latchup is being renewed with the evolution of complimentary metal-oxide semiconductor (CMOS) technology, metal-oxide-semiconductor field-effect transistor (MOSFET) scaling, and high-level system-on-chip (SOC) integration. Clear methodologies that grant protection from latchup, with insight into the physics, technology and circuit issues involved, are in increasing demand. This book describes CMOS and BiCMOS semiconductor technology and their sensitivity to present day latchup phenomena, from basic over-voltage and over-current conditions, single event latchup (SEL) and cable discharge events (CDE), to latchup domino phenomena. It contains chapters focusing on bipolar physics, latchup theory, latchup and guard ring characterization structures, characterization testing, product level test systems, product level testing and experimental results. Discussions on state-of-the-art semiconductor processes, design layout, and circuit level and system level latchup solutions are also included, as well as: latchup semiconductor process solutions for both CMOS to BiCMOS, such as shallow trench, deep trench, retrograde wells, connecting implants, sub-collectors, heavily-doped buried layers, and buried grids – from single- to triple-well CMOS; practical latchup design methods, automated and bench-level latchup testing methods and techniques, latchup theory of logarithm resistance space, generalized alpha (a) space, beta (b) space, new latchup design methods– connecting the theoretical to the practical analysis, and; examples of latchup computer aided design (CAD) methodologies, from design rule checking (DRC) and logical-to-physical design, to new latchup CAD methodologies that address latchup for internal and external latchup on a local as well as global design level. Latchup acts as a companion text to the author's series

of books on ESD (electrostatic discharge) protection, serving as an invaluable reference for the professional semiconductor chip and system-level ESD engineer. Semiconductor device, process and circuit designers, and quality, reliability and failure analysis engineers will find it informative on the issues that confront modern CMOS technology. Practitioners in the automotive and aerospace industries will also find it useful. In addition, its academic treatment will appeal to both senior and graduate students with interests in semiconductor process, device physics, computer aided design and design integration.

The ESD Control Program Handbook Springer Science & Business Media

Revised and fully updated, the second edition of this graduate textbook offers a comprehensive explanation of the technology and physics of LEDs such as infrared, visible-spectrum, ultraviolet, and white LEDs made from III-V semiconductors. Elementary properties such as electrical and optical characteristics are reviewed, followed by the analysis of advanced device structures. With nine additional chapters, the treatment of LEDs has been vastly expanded, including new material on device packaging, reflectors, UV LEDs, III-V nitride materials, solid-state sources for illumination applications, and junction temperature. Radiative and non-radiative recombination dynamics, methods for improving light extraction, high-efficiency and high-power device designs, white-light emitters with wavelength-converting phosphor materials, optical reflectors, and spontaneous recombination in resonant-cavity structures are discussed in detail. With exercises, solutions, and illustrative examples, this textbook will be of interest to scientists and engineers working on LEDs and graduate students in electrical engineering, applied physics, and materials science.

Electrostatic Discharge Protection John Wiley & Sons

With the evolution of semiconductor technology and global diversification of the semiconductor business, testing of semiconductor devices to systems for electrostatic discharge (ESD) and electrical overstress (EOS) has increased in importance. ESD Testing: From Components to Systems updates the reader in the new tests, test models, and techniques in the characterization of semiconductor components for ESD, EOS, and latchup. Key features: Provides understanding and knowledge of ESD models and specifications including human body model (HBM), machine model (MM), charged device model (CDM), charged board model (CBM), cable discharge events (CDE), human metal model (HMM), IEC 61000-4-2 and IEC 61000-4-5. Discusses new testing methodologies such as transmission line pulse (TLP), to very fast transmission line pulse (VF-TLP), and future methods of long pulse TLP, to ultra-fast TLP (UF-TLP). Describes both conventional testing and new testing techniques for both chip and system level evaluation. Addresses EOS testing, electromagnetic compatibility (EMC) scanning, to current reconstruction methods. Discusses latchup characterization and testing methodologies for evaluation of semiconductor technology to product testing. ESD Testing: From

Components to Systems is part of the authors' series of books on electrostatic discharge (ESD) protection; this book will be an invaluable reference for the professional semiconductor chip and system-level ESD and EOS test engineer. Semiconductor device and process development, circuit designers, quality, reliability and failure analysis engineers will also find it an essential reference. In addition, its academic treatment will appeal to both senior and graduate students with interests in semiconductor process, device physics, semiconductor testing and experimental work.

Electrical Overstress (EOS) Cambridge University Press

The book all semiconductor device engineers must read to gain a practical feel for latchup-induced failure to produce lower-cost and higher-density chips. Transient-Induced Latchup in CMOS Integrated Circuits equips the practicing engineer with all the tools needed to address this regularly occurring problem while becoming more proficient at IC layout. Ker and Hsu introduce the phenomenon and basic physical mechanism of latchup, explaining the critical issues that have resurfaced for CMOS technologies. Once readers can gain an understanding of the standard practices for TLU, Ker and Hsu discuss the physical mechanism of TLU under a system-level ESD test, while introducing an efficient component-level TLU measurement setup. The authors then present experimental methodologies to extract safe and area-efficient compact layout rules for latchup prevention, including layout rules for I/O cells, internal circuits, and between I/O and internal circuits. The book concludes with an appendix giving a practical example of extracting layout rules and guidelines for latchup prevention in a 0.18-micrometer 1.8V/3.3V silicided CMOS process. Presents real cases and solutions that occur in commercial CMOS IC chips Equips engineers with the skills to conserve chip layout area and decrease time-to-market Written by experts with real-world experience in circuit design and failure analysis Distilled from numerous courses taught by the authors in IC design houses worldwide The only book to introduce TLU under system-level ESD and EFT tests This book is essential for practicing engineers involved in IC design, IC design management, system and application design, reliability, and failure analysis. Undergraduate and postgraduate students, specializing in CMOS circuit design and layout, will find this book to be a valuable introduction to real-world industry problems and a key reference during the course of their careers.

ESD Design Challenges and Strategies in Deeply-scaled Integrated Circuits Springer Science & Business Media

This book addresses key aspects of analog integrated circuits and systems design related to system level electrostatic discharge (ESD) protection. It is an invaluable reference for anyone developing systems-on-chip (SoC) and systems-on-package (SoP), integrated with system-level ESD protection. The book focuses on both the design of semiconductor integrated circuit (IC) components with embedded, on-chip system level protection and IC-system co-design. The readers will be enabled to bring the system level ESD protection solutions to the level of integrated circuits, thereby reducing or completely eliminating the need for additional, discrete components on the printed circuit board (PCB) and meeting system-level ESD requirements. The authors take a systematic approach, based on IC-system ESD protection co-design. A detailed description of the available IC-level ESD testing methods is provided, together with a discussion of the correlation between IC-level and system-level ESD testing methods. The IC-level ESD protection design is demonstrated with representative case studies which are analyzed with various

numerical simulations and ESD testing. The overall methodology for IC-system ESD co-design is presented as a step-by-step procedure that involves both ESD testing and numerical simulations.

ESD John Wiley & Sons

Based on the authors' expansive collection of notes taken over the years, Nano-CMOS Circuit and Physical Design bridges the gap between physical and circuit design and fabrication processing, manufacturability, and yield. This innovative book covers: process technology, including sub-wavelength optical lithography; impact of process scaling on circuit and physical implementation and low power with leaky transistors; and DFM, yield, and the impact of physical implementation.

Simulation Methods for ESD Protection Development Springer Science & Business Media

This Book and Simulation Software Bundle Project Dear Reader, this book project brings to you a unique study tool for ESD protection solutions used in analog-integrated circuit (IC) design. Quick-start learning is combined with in-depth understanding for the whole spectrum of cro-disciplinary knowledge required to excel in the ESD ?eld. The chapters cover technical material from elementary semiconductor structure and device levels up to complex analog circuit design examples and case studies. The book project provides two different options for learning the material. The printed material can be studied as any regular technical textbook. At the same time, another option adds parallel exercise using the trial version of a complementary commercial simulation tool with prepared simulation examples. Combination of the textbook material with numerical simulation experience presents a unique opportunity to gain a level of expertise that is hard to achieve otherwise. The book is bundled with simpli?ed trial version of commercial mixed- TM mode simulation software from Angstrom Design Automation. The DECIMM (Device Circuit Mixed-Mode) simulator tool and complementary to the book s- ulation examples can be downloaded from www.analogesd.com. The simulation examples prepared by the authors support the speci?c examples discussed across the book chapters. A key idea behind this project is to provide an opportunity to not only study the book material but also gain a much deeper understanding of the subject by direct experience through practical simulation examples.

Transient-Induced Latchup in CMOS Integrated Circuits John Wiley & Sons

This book enables readers to design effective ESD protection solutions for all mainstream RF fabrication processes (GaAs pHEMT, SiGe HBT, CMOS). The new techniques introduced by the authors have much higher protection levels and much lower parasitic effects than those of existing ESD protection devices. The authors describe in detail the ESD phenomenon, as well as ESD protection fundamentals, standards, test equipment, and basic design strategies. Readers will benefit from realistic case studies of ESD protection for RFICs and will learn to increase significantly modern RFICs’ ESD safety level, while maximizing RF performance.

On-chip ESD Protection in Integrated Circuits John Wiley & Sons

The book gathers a collection of high-quality peer-reviewed research

papers presented at the International Conference on Information System Design and Intelligent Applications (INDIA 2018), which was held at the Universite des Mascareignes, Mauritius from July 19 to 21, 2018. It covers a wide range of topics in computer science and information technology, from image processing, database applications and data mining, to grid and cloud computing, bioinformatics and many more. The intelligent tools discussed, e.g. swarm intelligence, artificial intelligence, evolutionary algorithms, and bio-inspired algorithms, are currently being applied to solve challenging problems in various domains.

ESD in Silicon Integrated Circuits CRC Press

* Examines the various methods available for circuit protection, including coverage of the newly developed ESD circuit protection schemes for VLSI circuits. * Provides guidance on the implementation of circuit protection measures. * Includes new sections on ESD design rules, layout approaches, package effects, and circuit concepts. * Reviews the new Charged Device Model (CDM) test method and evaluates design requirements necessary for circuit protection.

Mixed-Signal Circuits John Wiley & Sons

Electrostatic discharge (ESD) is one of the most prevalent threats to electronic components. In an ESD event, a finite amount of charge is transferred from one object (i.e., human body) to another (i.e., microchip). This process can result in a very high current passing through the microchip within a very short period of time. Thus, more than 35 percent of single-event chip damages can be attributed to ESD events, and designing ESD structures to protect integrated circuits against the ESD stresses is a high priority in the semiconductor industry. Electrostatic Discharge Protection: Advances and Applications delivers timely coverage of component- and system-level ESD protection for semiconductor devices and integrated circuits. Bringing together contributions from internationally respected researchers and engineers with expertise in ESD design, optimization, modeling, simulation, and characterization, this book bridges the gap between theory and practice to offer valuable insight into the state of the art of ESD protection. Amply illustrated with tables, figures, and case studies, the text: Instills a deeper understanding of ESD events and ESD protection design principles Examines vital processes including Si CMOS, Si BCD, Si SOI, and GaN technologies Addresses important aspects pertinent to the modeling and simulation of ESD protection solutions Electrostatic Discharge Protection: Advances and Applications provides a single source for cutting-edge information vital to the research and development of effective, robust ESD protection solutions for semiconductor devices and integrated circuits.